REMARKS

In response to the Office Action mailed September 23, 2004, Applicant respectfully requests reconsideration.

Claims 6-10 were objected to as being misnumbered. Applicant has renumbered these claims as 6-11 and amended the dependencies of the dependent claims as appropriate. This amendment is for clarification only and in no way narrows the scope of the claims. Accordingly, withdrawal of the objection under 37 C.F.R. §1.126 is respectfully requested.

Claims 1-10 were rejection under 35 U.S.C. §102(e) as being anticipated by Callahan. Applicant respectfully disagrees with this rejection.

The Office Action suggests that column 5, lines 16-19 of Callahan describes the feature of using said set of target registers and said live range to ensure that target registers holding target addresses in a live state are not available for other uses. Applicant respectfully disagrees. This passage of Callahan states that the target register allocation system can place a target definition for a target register in the pre-header when the last branch of a family of live ranges that use that target register in the loop, and no other family that uses that target register, has a target definition located in the loop. The target register allocation system does so by extending the live range in the family to encompass the loop.

This disclosure in Callahan is not the same as ensuring that target registers holding target addresses in a live state are not available for other uses. Callahan is directed at minimizing the number of target definitions, for example, by identifying branches that have the same target and attempting to locate a target definition so that is can be shared by both branches (see col. 3, lines 51-62 of Callahan). The cited passage in Callahan is one aspect of this in relation to a loop. Column 3, lines 62-65 of Callahan go on to explain that if a branch is located within a loop, the target register allocation system attempts to move the target definition outside the loop so that the target register is not reloaded during each execution of a loop. By defining that "no other family that uses that target register has a target definition located in the loop", Callahan does not prevent the target register being available for other uses. This criterion merely determines whether the target register allocation system extends the live range in the family to encompass

the loop. The cited passage in Callahan discloses no method for blocking reuse of a target register between the steps of issuing a set branch instruction and an effect branch instruction.

Accordingly, nowhere does Callahan teach or suggest a method of compiling a computer program from a sequence of computer instructions including a plurality of first, set branch, instructions which each identify a target address for a branch and a plurality of associated second, effect branch instructions which each implement a branch to a target address, including, *inter alia*, using said set of target registers and said live range to ensure that target registers holding target addresses in a live state are not available for other uses. Claim 1 thus distinguishes over Callahan and is in allowable condition.

Claims 2-5 depend from claim 1 and are allowable for at least the same reasons.

Claim 6 recites a method of operating a computer system to compile a computer program from a sequence of computer instructions including a plurality of first, set branch instructions which each identify a target address for a branch and a plurality of second, effect branch instructions which each implement a branch to the target address specified in the associated set branch instruction, including, *inter alia*, executing a lifetime tracking algorithm to define as a live range of blocks a set of blocks for which a target address of a particular set branch instruction is in a live state, said lifetime tracking algorithm being operable to use said set of target registers and said live range to ensure that target registers holding target addresses in a live state are not available for other uses.

As discussed above in connection with claim 1, Callahan does not teach or suggest at least this limitation. Accordingly, claim 6 distinguishes over Callahan and is in allowable condition.

Claims 7 and 8 depend from claim 6 and are allowable for at least the same reasons.

Claim 9 recites a compiler for compiling a computer program from a sequence of computer instructions including a plurality of first, set branch instructions which each identify a target address for a branch and a plurality of associated second, effect branch instructions which implement a branch to the target address specified in the associated set branch instruction, comprising, *inter alia*, circuitry for executing a lifetime tracking algorithm which defines as a live range of blocks a set of blocks for which a target address of a particular set branch

instruction is in a live state, and which is arranged to use said set of target registers and said live range to ensure that target registers holding target addresses in a live state are not available for other uses.

As discussed above in connection with claim 1, Callahan clearly does not teach or suggest at least this limitation. Accordingly, claim 9 distinguishes over Callahan and is in allowable condition.

Claim 10 and 11 depend from claim 9 and are allowable for at least the same reasons.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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